

MX0535VPX LDMOS TRANSISTOR

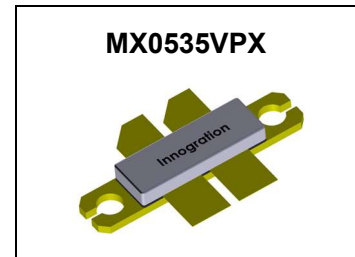
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Preliminary Datasheet V1.1

350W, 50V High Power RF LDMOS FETs

Description

The MX0535VPX is a 350-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 0.5 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.



- Typical performance(on 325MHz test board with device soldered):

$V_{DD} = 50$ Volts, $I_{DQ} = 200$ mA, CW.

Freq (MHz)	P3dB (W)	Gain (dB)	Eff (%)
325	380	16.2	67.3

- Typical performance(on 500MHz test board with device soldered):

$V_{DD} = 50$ Volts, $I_{DQ} = 200$ mA, CW.

Freq (MHz)	P3dB (W)	Gain (dB)	Eff (%)
500	363	13.3	67.4

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+135	Vdc
Gate--Source Voltage	V_{GS}	-9 to +11	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
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Thermal Resistance, Junction to Case $T_C=85^{\circ}\text{C}$, $T_J=200^{\circ}\text{C}$, DC test	$R_{\theta JC}$	0.25	$^{\circ}\text{C/W}$
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Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Voltage $V_{GS}=0$, $I_{DS}=1.0\text{Ma}$	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	---	---	1	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	---	---	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	---	---	1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$	---	2.65	---	V
Gate Quiescent Voltage ($V_{DD} = 50\text{V}$, $I_D = 200\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	---	3.35	---	V
Drain source on state resistance ($V_{ds}=0.1\text{V}$, $V_{gs}=10\text{V}$)	$R_{ds(on)}$		352		$\text{m}\Omega$
Common Source Input Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 50\text{V}$, $f = 1\text{MHz}$)	C_{ISS}		141		pF
Common Source Output Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 50\text{V}$, $f = 1\text{MHz}$)	C_{OSS}		42		pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 50\text{V}$, $f = 1\text{MHz}$)	C_{RSS}		0.7		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 50\text{Vdc}$, $I_{DQ} = 200\text{mA}$, $f = 500\text{MHz}$, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 350W Pulsed CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram

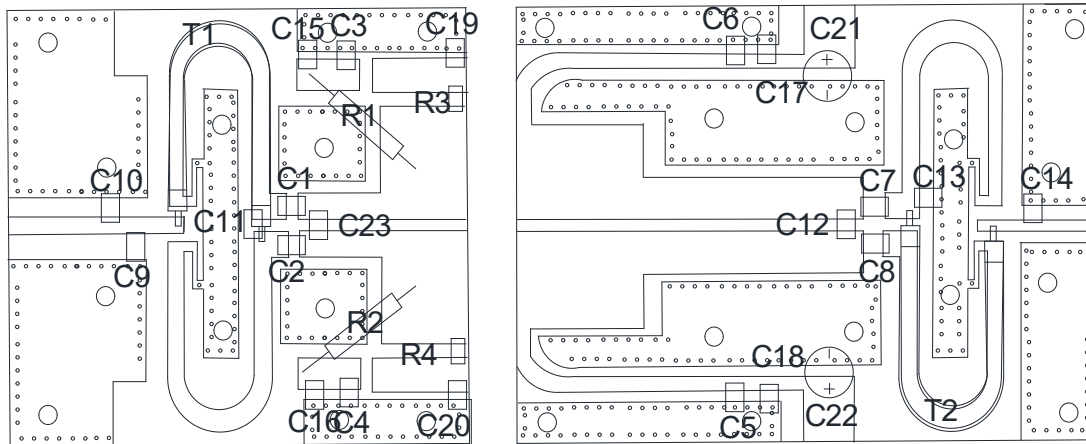


Figure 1. Test Circuit Component Layout (325M)

Table 1. Test Circuit Component Designations and Values (325M)

Part	description	Model
C1~C6	220PF	DLC70B
C13	3PF	DLC70B
C7, C8	100PF	ATC800B
C9	20PF	DLC70B
C10	1.5PF	DLC70B
C11	15PF	DLC70B
C12	12PF	DLC70B
C14	6.8PF	ATC800B
C15~c18	10UF	100V/10UF
C21, c22	470UF	63V/470UF
C23	18PF	DLC70B
R1	100Ω	
R2	16 Ω	1206
T1,T2	55mm	SF-86-25

TYPICAL CHARACTERISTICS

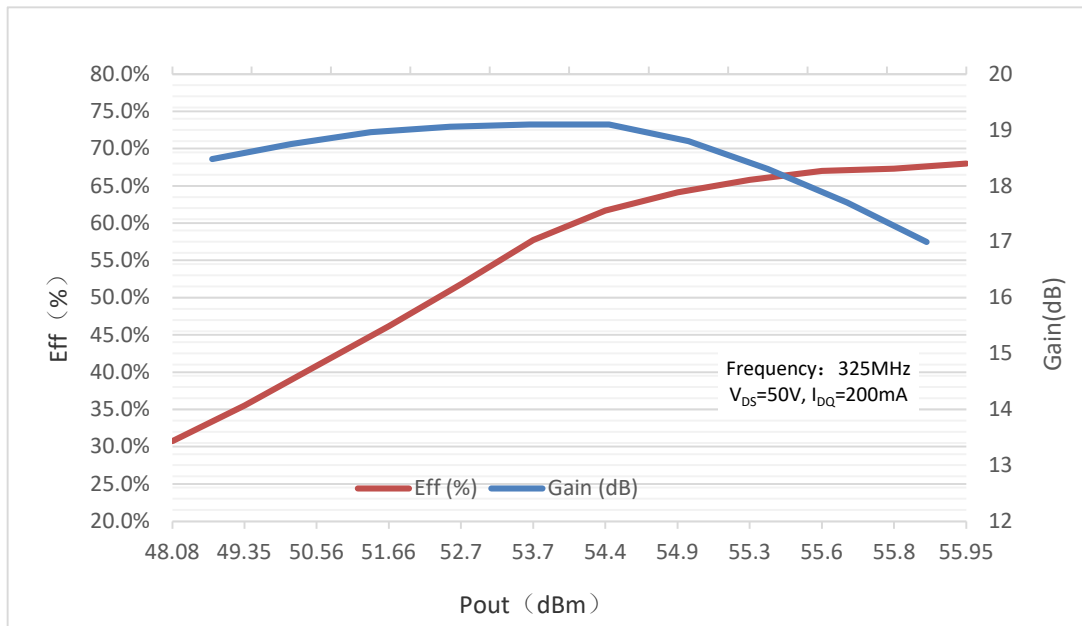


Figure 2: Power Gain and Drain Efficiency as Function of CW Power (325M)

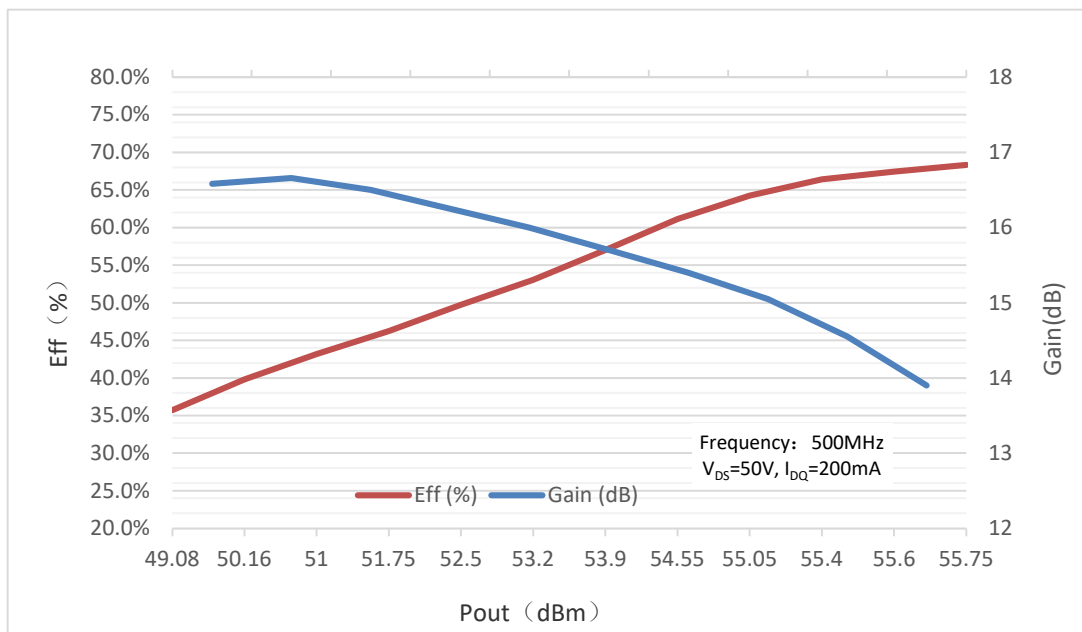


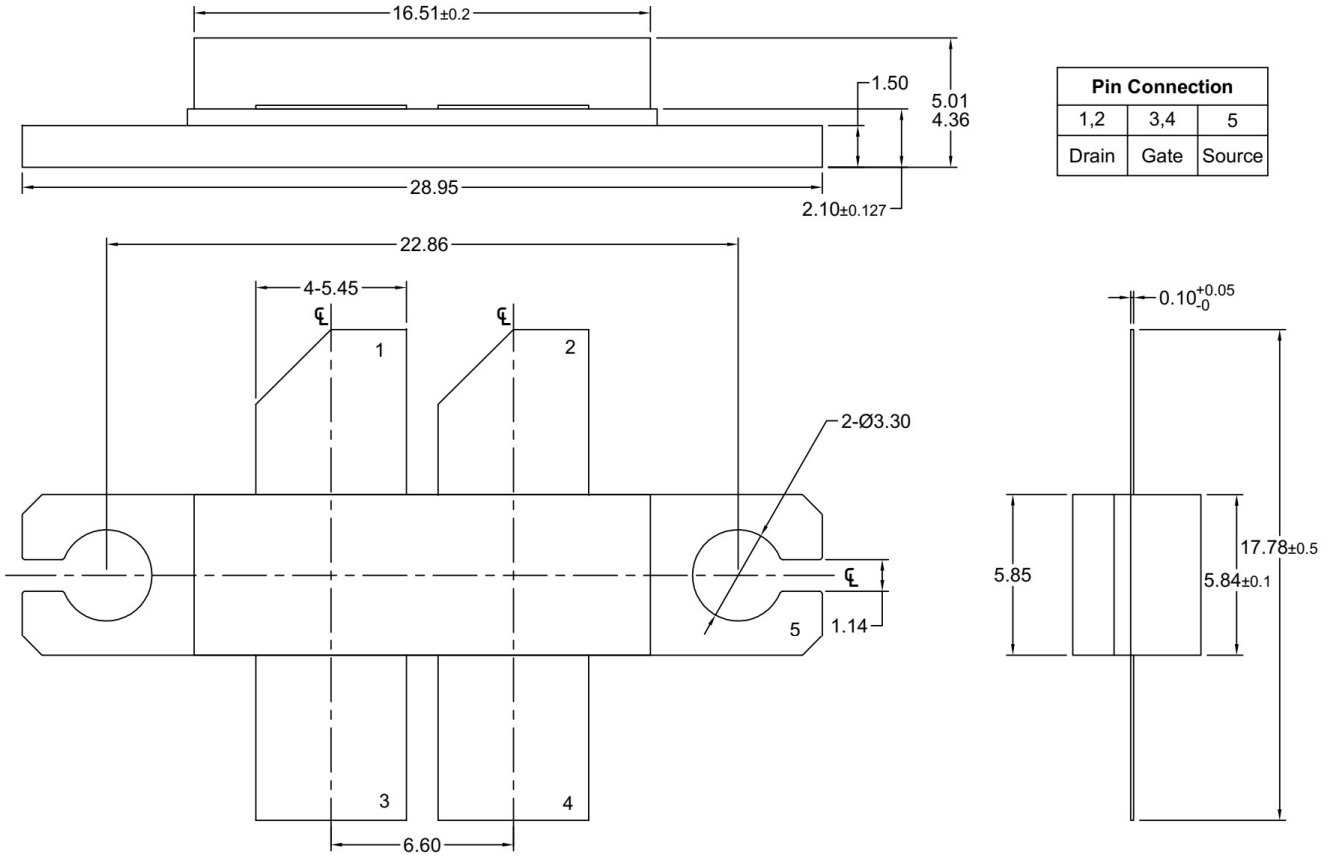
Figure 3: Power Gain and Drain Efficiency as Function of CW Power (500M)

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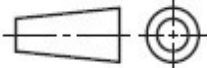
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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



Unit: mm
Tolerances (unless specified): x.x ±0.15
x.xx ±0.127

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LBB					11/15/2019

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Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2019/11/15	Rev 1.0	Preliminary Datasheet Creation
2024/7/6	Rev 1.1	Modify the typo of breakdown voltage

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