MQ0570VPX LDMOS TRANSISTOR

Document Number: MQ0570VPX
Preliminary Datasheet V1.2

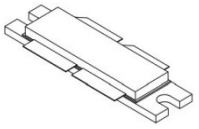
700W, 50V High Power RF LDMOS FETs

Description

The MQ0570VPX is a 700-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 500MHz. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

MQ0570VPX



- Typical Performance (On Innogration 100-400MHz wideband fixture with device soldered):

V_{DD} = 48 Volts, I_{DQ} = 200 mA, CW,

Freq (MHz)	Pin (dBm)	Psat (dBm)	Psat (W)	IDS (A)	Gain (dB)	Eff (%)	2nd Harmonic(dBc)	3rd Harmonic(dBc)
100	41.2	57.2	524.8	13.8	16	79.2	-15	-13
150	40.1	57.3	537.0	16.9	17.2	66.2	-24	-10
200	41.5	57.8	602.6	19.7	16.3	63.7	-25	-16
250	40.2	57.9	616.6	20.4	17.7	63.0	-20	-25
300	41	57.8	602.6	19.4	16.8	64.7	-29	-31
350	41.6	57.2	524.8	18.4	15.6	59.4	-33	-30
400	42.2	57	501.2	17.6	14.8	59.3	-35	-24

- Typical Performance (On Innogration 88-108MHz wideband fixture with device soldered):

V_{DD} = 48 Volts, I_{DQ} = 200 mA, CW,

Freq (MHz)	Pout (dBm)	Pout (W)	Ids (A)	Pin (dBm)	Gain (dB)	Eff (%)	SWR
87	57.80	602.6	16.20	35.70	22.10	77.49	1.39
98	58.45	699.8	18.20	35.60	22.85	80.11	1.09
108	58.42	695.0	19.03	36.30	22.12	76.09	1.39

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- On chip RC network enable high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	135	Vdc

Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 700W CW, 50 Vdc, I_{DQ} = 200 mA	$R_{\theta JC}$	0.13	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.04	°C/W

Table 3. ESD Protection Characteristics

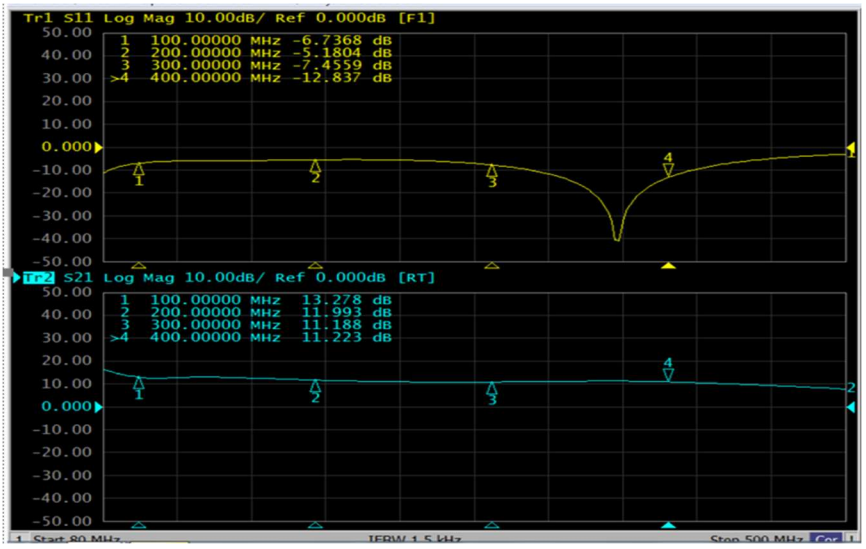
Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.68	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.0	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		180		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		280		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		80		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		1.5		pF

TYPICAL CHARACTERISTICS

Figure 1: Network analyzer output S11/S21 at 48V Idq=200mA



Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request, 30mil RO4350)

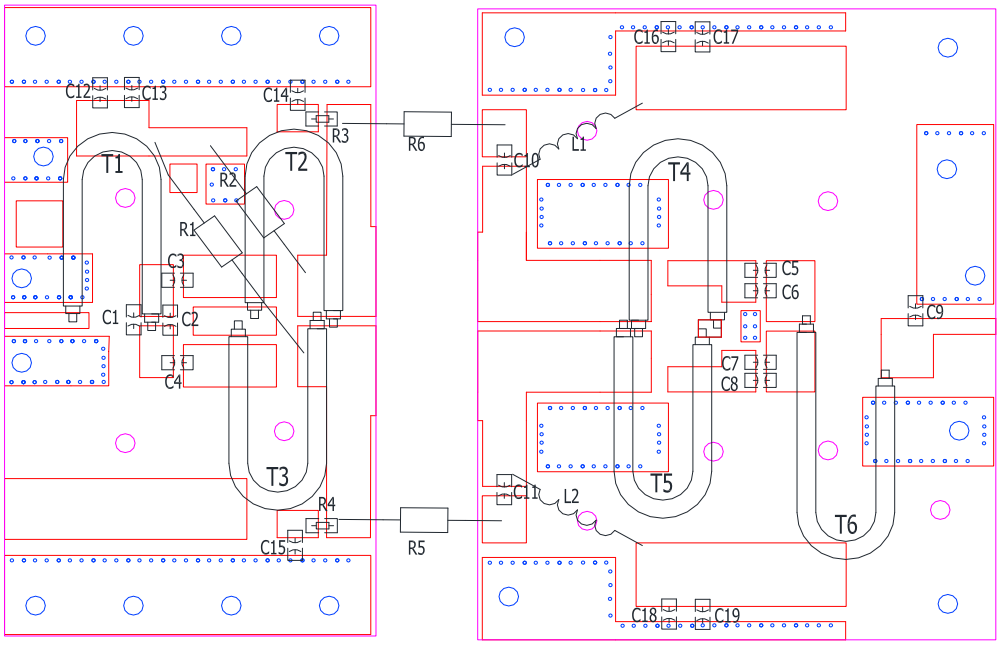


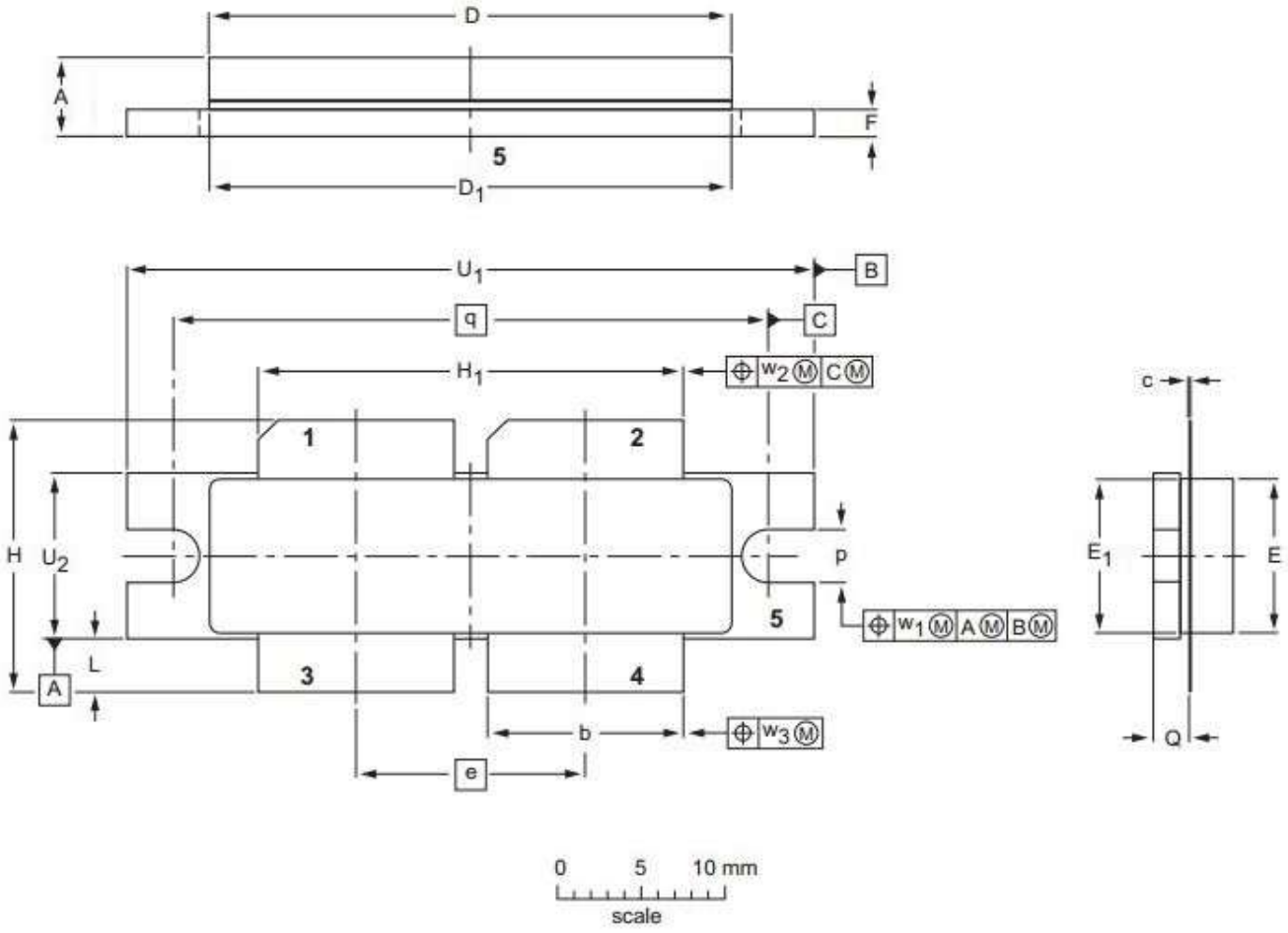
Table 5. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1	3.3pF	DLC70B
C2	8.2pF	ATC800B
C3,C4	200pF	DLC75D
C5,C6,C7,C8,C13,C14,C15,C16,C18	470pF	ATC800B
C9	1.8pF	DLC70B

C10,C11	82pF	DLC70B
C12,C17,C19	10uF	10uF/50V
R1,R2	470ohm	
R3,R4	Chip Resistor,5.1ohm	1206
R5,R6	200ohm	
T1	50ohm,70mm	SF-086-50
T2,T3	12.5ohm,70mm	SFF-12.5-1.5
T4,T5	12.5ohm,80mm	SFF-12.5-1.5
T6	50ohm,70mm	RG-402-3
L1,L2	6 turns,D=5mm	

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/2/22	Rev 1.0	Preliminary Datasheet
2021/3/25	Rev 1.1	Add 100-400MHz application data
2023/10/27	Rev 1.2	Add 88-108MHz application data

Application data based on ZL-21-07/TC-23-69

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